REMARKS

The Office Action dated March 19, 2003 has been received and carefully noted. The above amendment to the title and the following remarks, are submitted as a full and complete response thereto. Accordingly, Applicant requests the favorable consideration of claims 1-19.

The title of the invention is objected to. The title is amended to more clearly describe the invention. Accordingly, Applicants request the withdrawal of the objection to the Title.

The Office Action rejected claim 1 under 35 U.S.C. §103(a) as being unpatentable over the Applicant Admitted Prior Art (APA) (Figures 24, 25, 26, 27, 28) in view of Yin (US Patent No. 5635737). The Office Action takes the position that the combination of the APA and Yin teach or suggest all the features recited in claims 1-19. Applicants respectfully disagree.

Claim 1 is directed to a semiconductor integrated circuit device. A pair of a first power wiring and a second power wiring are arranged in one direction. A first region is provided between the first power wiring and the second power wiring. A fundamental circuit units are constituted by combining one or more PMOS transistors and one or more NMOS transistors. The fundamental circuit units are arranged along with the first power wiring and the power wiring. Logic circuit units are constituted by a plurality of the fundamental circuit units. Functional circuit units are constituted by a plurality of the logic circuit units. The functional circuits are connected to each other and at least one part of the PMOS transistors and that of the NMOS transistors are arranged below the first wiring and the second power wiring. Unit connection wirings are used to connect between the fundamental circuit units or to connect between the logic circuit units, of which the terminals terminate at the functional circuit and are arranged on second regions that are other than the first region. In case the unit connection wirings are constituted by a layer that is same as a wiring layer that constitutes the first power wiring and the second power wiring or by wiring layers that are under the wiring layer of the first and second power wirings.

The Applicant Admitted Prior Art (APA) (Figures 24-28) illustrate layout patterns of logic circuits that are conventional. However, the APA, as admitted by the Office Action,

does not teach or suggest unit connection wirings used to connect between the fundamental circuit units or to connect between the logic circuit units, of which the terminals terminate at the functional circuit and are arranged on second regions that are other than the first region. In case the unit connection wirings are constituted by a layer that is same as a wiring layer that constitutes the first power wiring and the second power wiring or by wiring layers that are under the wiring layer of the first and second power wirings.

Yin is directed to improvement in gate array technology which enhances the testability of the gate array by improving the difficulty in testing of all of the output of the gate array on a CMOS logic gate array as well as to solve density problems. Yin discloses a complementary metal-oxide silicon logic gate and a CMOS logic gate array having a plurality of core cells. Yin also discloses a testability area. The testability area includes a plurality of probe lines located between transistor pairs. The probe lines include pad members to facilitate testing of the outputs for the gate array. More specifically, a gate array structure 150 includes two core cells 100 and a testability area 250. Yin also discloses that the testability area 250 is located between the active area of the two cells 100 and that the testability area 250 comprises a probe line 252 to facilitate the connection to the output and pad members 254.

However, Yin does not teach or suggest unit connection wirings to connect between the fundamental circuit units or to connect between the logic circuit units, of which terminals terminate at the functional circuit units are arranged on second regions that are other than the first region, in case the unit connection wirings are constituted by a layer that is same as a wiring layer that constitutes the first power wiring and the second power wiring or by wiring layers that are under the wiring layer of the first and second power wirings. As mentioned above, Yin is merely directed to enhancing the testability of the gate array.

In other words, it is submitted that Yin does not cure the deficiencies of the APA. It should be noted that Yin intends to improve the testability of the gate array, and to secure the testability area 250 for wiring of a probe line 252. Whereas, the claimed invention is related to layout patters to arrange a plurality of function circuits provided with a plurality of logical circuit in a single direction along with the flow of signals, which is set to meet demands on higher integration design of a die size of a semiconductor integrated circuit

device. In addition, the wirings between circuits in the claimed invention are connected on a layer of a power wiring or on a wiring layer below the layer of the power wiring so that a signal can flow along with the power wiring. In contrast, Yin as shown in Figure 4, illustrates a probe line 252, and the power lines crossed orhthogonally. As is apparent from the above analysis, the applied references taken either singly or in combination do not teach or suggest unit connection wirings to connect between the fundamental circuit units or to connect between the logic circuit units, of which terminals terminate at the functional circuit units are arranged on second regions that are other than the first region, in case the unit connection wirings are constituted by a layer that is same as a wiring layer that constitutes the first power wiring and the second power wiring or by wiring layers that are under the wiring layer of the first and second power wirings. Accordingly, Applicant respectfully requests the withdrawal of the rejection of claim 1.

Claims 1-19 are dependent upon claim 1, therefore these claims for at least the reasons mentioned above, recite features that are neither taught nor suggested by the applied prior art. Accordingly, Applicant respectfully requests the withdrawal of the rejection of claims 1-19.

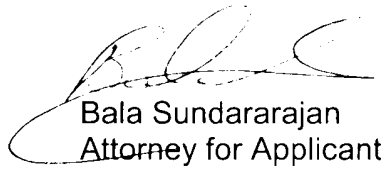
In view of the distinctions discussed above, withdrawal of the rejections to claims 1-19 is respectfully requested. No new matter is presented. Applicant submit claims 1-19 recite subject matter that is neither taught nor suggested by the applied references. Therefore, Applicant submits that the application is now in condition for allowance with claims 1-19 contained therein.

Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



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Enclosure: Petition for Extension of Time